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What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of fabricating a portion of a memory cell, said method comprising:

forming an insulating layer over a substrate;

forming a trench in said insulating layer;

lining said trench with a first barrier layer to a first conductive material;

forming said first conductive layer in said trench;

planarizing an upper surface of said layers;

forming a layer of a second conductive material over said layers; and

removing an upper portion of said second conductive layer to flatten an upper surface of said second conductive layer while leaving a lower portion of said second conductive layer intact over said first conductive layer.

2. The method of claim 1 wherein said first barrier layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

3. The method of claim 1 wherein said second conductive layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

4. The method of claim 1 wherein said second conductive layer is a resistive material.

5. The method of claim 1 wherein said first and second conductive layers are selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

6. The method of claim 1 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

7. The method of claim 1 wherein said first barrier layer is formed to a thickness of about 5 nm to about 10 nm.

8. The method of claim 1 wherein said second conductive layer is formed to a thickness of about 5 nm to about 20 nm.

9. The method of claim 1 wherein said upper portion of said second conductive layer is removed by chemical mechanical polishing.

10. A method of fabricating a portion of a memory cell, said method comprising:

forming a first conductor in a trench provided in an insulating layer;

flattening an upper surface of said insulating layer and said first conductor, said flattening leaving a roughened upper surface of said conductor;

forming a material layer over said flattened upper surface of said insulating layer and said first conductor; and

flattening an upper portion of said material layer while leaving intact a lower portion of said material layer over said insulating layer and said first conductor.

11. The method of claim 10 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

12. The method of claim 10 wherein said material layer is a resistive material.

13. The method of claim 10 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

14. The method of claim 10 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

15. The method of claim 10 wherein said upper portion of said material layer is flattened by chemical mechanical polishing.

16. A method of fabricating a portion of a memory cell, said method comprising:

forming a first conductor layer over an insulating layer of a substrate;

flattening an upper surface of said layers, said flattening leaving a roughened upper surface of said conductive layer;

forming a material layer over said flattened upper surface of said layers; and

flattening an upper portion of said material layer while leaving intact a lower portion of said material layer over said conductive layer.

17. The method of claim 16 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

18. The method of claim 16 wherein said material layer is a resistive material.

19. The method of claim 16 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

20. The method of claim 16 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

21. The method of claim 16 wherein said upper portion of said material layer is flattened by chemical mechanical polishing.

22. A magnetic random access memory structure comprising:

a plurality of longitudinally extending planarized conductive lines formed over an insulating layer of a semiconductor substrate;

respective first magnetic layers over said conductive lines;

respective second magnetic layers over said first magnetic layers;

at least one contact; and

a planarized conductive material layer formed between said planarized conductive lines and said first magnetic layers.

23. The structure of claim 22 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

24. The structure of claim 22 wherein said material layer is a resistive material.

25. The structure of claim 22 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

26. The structure of claim 22 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

27. The structure of claim 22 wherein said conductive lines are formed in a trench formed in said substrate.

28. A memory device comprising:

at least one magnetic random access memory cell, said magnetic random access memory cell comprising a first ferromagnetic layer formed over a first planarized conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a planarized conductor layer provided between said first conductor and said first ferromagnetic layer.

29. The device of claim 28 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

30. The device of claim 28 wherein said material layer is a resistive material.

31. The device of claim 28 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 or polyimide.

32. The device of claim 28 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

33. The device of claim 28 wherein said first conductor is formed in a trench of a substrate.

34. A processor-based system, comprising:

a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a plurality of magnetic random access memory cells, each of said magnetic random access memory cells including a first ferromagnetic layer formed over a first planarized conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a planarized conductor layer provided between said first conductor and said first ferromagnetic layer.

35. The system of claim 34 wherein said material layer is selected from the group consisting of tantalum (Ta), titanium (Ti), titanium-tungsten (TiW), titanium nitride (TiN) and chromium (Cr).

36. The system of claim 34 wherein said material layer is a resistive material.

37. The system of claim 34 wherein said insulating layer is selected from the group consisting of BPSG, SiO, SiO_2, Si_3N_4 and polyimide.

38. The system of claim 34 wherein said material layer is formed to a thickness of about 5 nm to about 20 nm.

39. The system of claim 34 wherein said first conductor is formed in a trench of a substrate.